

## VHDL Templates

This is a quick crib sheet for understanding vhd templates in emacs. It assumes that you have emacs running, in vhd-mode and that you have an empty file to play with. ( or use the and2 example)

When you type in a keyword, or select from the templates submenu, you will be prompted for input at each stage. To abandon a template just hit enter on an empty field. The following should all be done in emacs.

type C-c C-t en

This will start a template that looks like ...



```
Buffers Files Tools Edit Search Mule Minibuf Help
entity <name>
--:** dummy.vhd (VHDL/es)--L1--A11-----
name: |
```

It will enter the keyword for you, put a marker in in red text, move the cursor to the minibuffer at the bottom and wait for you to type in the entity name. When you have typed in the name, eg and2, hit enter. Emacs will then look like



```
Buffers Files Tools Edit Search Mule Minibuf Help
entity and2 is
generic (
  <[name]>
end and2;
--:** dummy.vhd (VHDL/es)--L4--A11-----
[name]: |
```

We are not using generics at this stage so just hit return to abandon this sub-template. You will then see (overleaf) the template for entering the port description which will expect you, in sequence, to enter the name(s) of the port(s) followed by [enter], the direction of the port [enter], the type of the port [enter] and then a comment [enter]. At each stage the cursor will move to the minibuffer and wait for input. If there is a limited selection, as with direction, it will show you the choices.

```
Buffers Files Tools Edit Search Mule Minibuf Help
entity and2 is
    port (
        <[names]>
    end and2;

--:** dummy.vhd (VHDL/es)--L4--All-----
[ names]:
```

port template

```
Buffers Files Tools Edit Search Mule Minibuf Help
entity and2 is
    port (
        x,y : <IN | OUT | INOUT>
    end and2;

--:** dummy.vhd (VHDL/es)--L4--All-----
IN | OUT | INOUT: in
```

direction template

```
Buffers Files Tools Edit Search Mule Minibuf Help
entity and2 is
    port (
        x,y : in <type>
    end and2;

--:** dummy.vhd (VHDL/es)--L4--All-----
type: bit
```

type template

```
Buffers Files Tools Edit Search Mule Minibuf Help
entity and2 is
  port (
    x,y : in bit;
  end and2;
  -- <[comment]>
--:** dummy.vhd (VHDL/es)--L4--A11-----
[comment]:
```

comment template

```
Buffers Files Tools Edit Search Mule Minibuf Help
entity and2 is
  port (
    x,y : in bit;
    z : out bit;
    <[names]>
  end and2;
--:** dummy.vhd (VHDL/es)--L6--A11-----
[names]:
```

completed entity, hit enter on empty name field to end.

```
Buffers Files Tools Edit Search Mule Minibuf Help
entity and2 is
  port (
    x, y : in bit;
    z : out bit);
  end and2;
  architecture <name>
--:** dummy.vhd (VHDL/es Abbrev)--L9--A11-----
name:
```

start of architecture template