

Note that some of the sample questions come from older papers that had different marks weightings. However the relative importance of each part of a question is consistent.

4) Your employer, *Smart Lights International*, designs and manufactures custom lighting sequencers and controllers. Currently they use a traditional approach incorporating microcontrollers, or microprocessors, with programs written in a mixture of C and assembler. Having been sent on an introductory VHDL course, you are expected to write a report assessing the advantages and disadvantages to the company of using VHDL combined with 'in system' programmable logic devices.

a) Explain what software and hardware tools are required in principle, in order that a design may be taken from an initial idea to the target hardware. Assume that VHDL will be used and that the target is a CPLD (Complex Programmable Logic Device). Your explanation should make reference to the role played by each tool.

(4 Marks)

b) Briefly discuss the issues involved in developing, simulating and implementing hardware designs using VHDL from both hardware and software design perspectives.

(6 marks)

c) Explain, with respect to VHDL simulation, what is meant by the terms δ delay (delta) and inertial delay.

(2 Marks)

d) Explain, with the aid of timing diagrams, how a VHDL simulator would execute the following fragment of behavioural code and show when the transactions are placed on the signals :-

```
ARCHITECTURE timing OF exam IS
    SIGNAL a,b,c : BIT := '0';
BEGIN
    a <= '1' AFTER 15NS;
    b <= NOT a after 5NS;
    c <= a AFTER 10NS;
END timing;
```

(8 Marks)

3) Designers are increasingly using high level languages such as VHDL, followed by logic synthesis to develop systems. Implementation is achieved by using technologies such as ASICs, FPLDs or CPLDs.

a) Discuss the advantages and disadvantages facing a designer when using a high level languages such as VHDL to design a system and implement it in the target hardware. You may use examples from your assignment work in your discussion. You should include consideration of the tools used and tool-chain compatibility issues.

(20 Marks)

b) Explain how the description and synthesis of a finite state machine in VHDL differs from a software description of a finite state machine in a language such as C. Your answer should include a discussion of the difficulties faced by a software engineer when first working with VHDL.

(13 Marks)

4) A television game show requires a control system for managing the contestants buzzers. The requirements are

The game show has three contestants *A*, *B* and *C*. Each player has a signalling button which goes to a circuit that outputs *YZ*. The circuit sets *YZ* to 00 when no player has pressed a button, and sets *YZ* = 01, 10 or 11 respectively when the first player to press the signalling button is player *A*, *B* or *C* respectively. A clue is displayed and one of the players presses the signalling button; this locks out the other players from being recognized, and activates the signallers output light, A_o , B_o or C_o . If the answer is correct, the host presses the *R* button (right/reset), enabling all the players buttons. If not, the host presses the *W* (wrong) button. This disables that players button, turns off their light and

reenables the remaining players buttons. They can ring in and are processed in the same manner. (Thus, if a second players answer is wrong then only the third players button is enabled.) At any time that no player is answering a question, the host can reset the game by pressing the *R* button, for example, when time expires. [from *J. Carpinelli, 2001*].

- a) Provide a list of events and actions derived from the specification given above.
(5 marks)
- b) Develop either
a state table for the game show controller, this should show current state, events, actions and next state.

OR

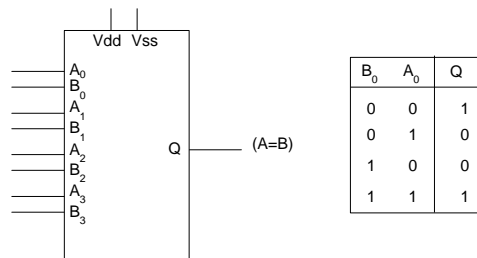
a state diagram for a Mealy state machine showing state names, transitions, events and actions.

(20 marks)

- c) Explain how you might implement your state machine using a ROM lookup table. You may use diagrams and/or fragments of VHDL code.

(8 marks)

- 4) The following block diagram represents a 4-bit equality comparator. It takes 2, 4-bit inputs and provides a 'TRUE' output when both sets of inputs are equal. This is shown in the accompanying truth table for bits A0 and B0



Provide a logic circuit diagram for the truth table and demonstrate how this would be extended to provide the comparator shown above .

(8 Marks)

- b) Use the components given in appendix (1) to create a structural VHDL model of the comparator. Develop intermediate components where appropriate.

(12 marks)

Appendix 1: STANDARD-CELL LIBRARY

NAME

a2_y

DESCRIPTION

-Interface

```
entity a2_y is
  port(
    i0 : in bit;
    i1 : in bit;
    t  : out bit;
    vdd : in bit;
    vss : in bit);
```

description-Logical

```
t <= (i0 and i1);
```

NAME

o2_y

DESCRIPTION

-Interface

```
entity o2_y is
  port(
    i0 : in bit;
    i1 : in bit;
    t  : out bit;
    vdd : in bit;
    vss : in bit);
```

description-Logical

```
t <= (i0 or i1);
```

NAME

n1_y

DESCRIPTION

-Interface

```
entity n1_y is
  port(
    i : in bit;
    f : out bit;
    vdd : in bit;
    vss : in bit);
```

description-Logical

```
f <= not i;
```