

Delta delays in simulation

VHDL defines a number of delay types which were discussed elsewhere. For simulation purposes a delay, known as δ (delta) delay is required when we wish to model hardware concurrency. The following example is from Navabi, VHDL, Analysis and Modelling of Digital Systems.

```
ENTITY timing IS
  (PORT(a,b : IN BIT; z,zbar : OUT BIT);
END ENTITY;

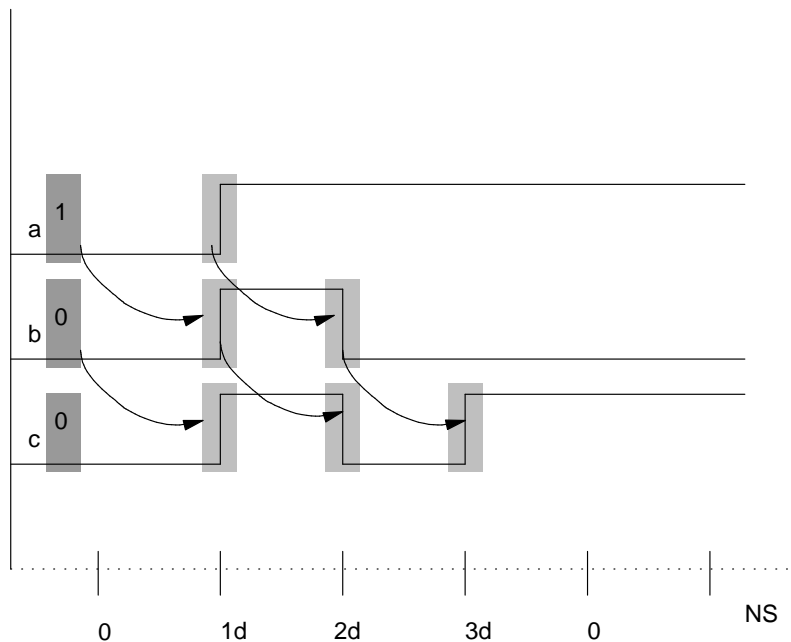
ARCHITECTURE delta of timing IS
BEGIN
  zbar <= NOT z;
  z <= a AND b AFTER 10 NS;
END delta;
```

When an event occurs on inputs a or b, a AND b is evaluated and scheduled to appear on z after 10ns. As this is a concurrent system the value of A AND B and its compliment should appear at the same time. However we cannot calculate the compliment until we know the value of z. To hide this waiting, VHDL uses the concept of δ time, in which it calculates the new value and then displays it.

In this example z receives its new signal 10ns after an event on a or b. zbar receives its new value after 10ns + δ . As delta time is only valid internal to the simulator, it appears that z and zbar have received their values at the same time.

A Further Example:

```
ARCHITECTURE concurrent OF timing_demo IS
BEGIN
  a <= '1';
  b <= NOT a;
  c <= NOT b;
END concurrent;
```



Here it can be seen that The initial state of the system is available at 0ns + 3 δ .

