



MODULAR PROGRAMME
ASSESSED COURSE-WORK SPECIFICATION

Module Details:

Module Code: UFEEMY-20-3	Module Title: Embedded Co-design with C & VHDL	
Module Leader: Nigel Gunton		
Module Tutors: Nigel Gunton Craig Duffy		
Assignment CW1	Element Number: Weighting 1 : 60%	Total Assignment Time: 29 hrs + lab time

Dates:

Date assignment issued to students: w/b 29th Oct.07	Date for return of marked work: w/b 22nd May 08
Submission Place: post-box in N foyer, below the North stairs	Date of Submission: 28th April.08
	Time of Submission: 14.00

Deliverables:

As listed on the Assignment spec sheet

Overview :

This assignment will provide experience of the problems and decisions in developing co-design projects. There are many possible solutions to the design problems depending on the way in which you choose to partition each problem.

The marks shown below are indicative and may be subject to modification during the year. This is because the proposed problem is potentially complex and may involve the use of the new TS7300 embedded board. We have not used this board before and there may be unforeseen challenges. You may choose to use the older Excalibur boards for the assignment, but you will be expected to deliver a working system.

You will develop a portfolio of documentation and results which will comprise the assignment deliverables. The deliverables are further defined below. Marks will be allocated across all design problems. To obtain 40% you would have to have completed an analysis of at least one of the problems along with implementation of at least part of the software/hardware required. To obtain 70%++ you would have to have completed most of the requirements and made significant progress in the others, the more progress, the greater the ++. The exact marks attribution is subject to variation due to the inherent difficulties in working with temperamental hardware.

1. Problem 1:

To design and implement a 'pick and place' system. A robot arm will be trained to move an item from one location to another. The training and control input will be from a 4x4 keypad. The arm has four independent servomotors. The software and hardware control will be implemented on either the Excalibur board or the TS7300. A different approach will be required for each board.

Excalibur Board:

This board has an APEX20KE FPGA fitted. This supports a 'soft-core' processor integrated with custom hardware. Using the Nios softcore CPU as a base you will implement a system to control a robot arm. The work will be done in small teams of 3±1. You will be required to partition the problem into suitable hardware and software units, integrate these units into a complete system and test. The documentation should show justification for any design decisions that you make as well as development logs for both hardware and software.

TS7300 Board:

This board has an ARM 9 based microcontroller and a CycloneII FPGA. There is an interface between the 2 devices. The ARM is running Debian GNU/Linux. The design requirements are the same, however you have full O/S support for the software. You are still required to use the keypad for input.

At a minimum your documentation for Problem 1 should include at least the following.

- An overview of your complete system including partitioning information.
- A list of the team members along with their roles and responsibilities, (to include authorship details of hardware & software components).
- An appendix containing your standards reference manual.
- Verification and testing strategies with results.
- Schematics and code outlines (VHDL, Verilog or C) for your components.

The Robot Arm :

An image and overview of the servo operation can be found at

http://www.cems.uwe.ac.uk/~ngunton/images/open_day_servo.pdf

The Key-Pad :

Data-sheet details for the keypad at

<http://www.cems.uwe.ac.uk/~ngunton/images/keypad.png>

The Design Problem :

The goal of this section is to develop a 'pick and place' system with training capabilities. A robot arm will be driven by manual control in order to define the waypoints for the place and pick. Once trained, the arm should automatically follow the programmed path on receipt of a run command.

Excalibur:

To develop a system, based around the Nios CPU, to control all four servos on the EMU robot arm. Input to the system is to be obtained from the provided keypad. The existing DIP switches and push buttons may be used for additional input if necessary. The LCD screen, the 2 seven segment displays and the LEDs must be used for user feedback.

or

TS7300:

The goal is to develop a standalone system. The final system must not rely on remote access to the board. You must integrate the keypad and the LCD screen to the board. All input must be via the keypad and display output must be to the LCD screen. You may also use the LEDs as user feedback. You may use the available onboard memory.

Using IP.

The use of pre-existing software or softcore IP is permitted. Any IP so used must be clearly attributed. In this instance the deliverables must include documentation explaining the function of the IP as well as any modifications that may have been made as part of the integration process.

Deliverables :

NOTE:

Marks distribution is indicative of the relative weighting of the components within this section but may be subject to change in the event of unexpected technical problems. The marks will be distributed across the two problems

- Design and development documentation which must include
 - Discussion of design partitioning and justification for your partitioning in problem 1. 15%
 - Your final hardware design, the marks indicated are shared between the problems.
 - i) Design 10%
 - ii) Implementation of components 10%
 - Your final software design, again marks are shared.
 - i) Design 15%
 - Change logs for Hardware and Software development 5%
 - Verification and Testing
 - i) Strategies for individual components and whole system. 10%
 - ii) Results 5%
- A viva and lab demonstration of the components and system for the problem that you have achieved the most with. 30%

NOTE:

The lab demos etc will take place during the last 2 lab sessions of the semester or sooner by arrangement.