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UWE BRISTOL

MODULAR PROGRAMME
ASSESSED COURSE-WORK SPECIFICATION

Module Details:

Module Code: **UFEEJ7-10-3**	Module Title: **VHDL for Real-time Systems**	
Module Leader: **Nigel Gunton**		
Module Tutors: **Nigel Gunton**		
Assignment **CW1**	Element Number: Weighting **75%**	Total Assignment Time: **12 hrs + lab time**

Dates:

Date assignment issued to students: **w/b 28rd Jan.**	Date for return of marked work: **w/b ?? May**
Submission Place: **post-box in N foyer, below the North stairs**	Date of Submission: **w/b 02 May.**
	Time of Submission: **10.00am**

Deliverables:

As listed on the Assignment spec sheet

Overview:

This assignment is designed to give you experience in the design, development and integration of custom hardware into an existing system. Due to time constraints we will simplify the process, the design phase will therefore focus on deriving a model from existing designs, rather than developing from scratch. Porting, in other words. However you will still need a thorough and detailed understanding of the design.

You will be developing a simple VGA interface for eventual integration into an existing system. In phase 1 you will create a 'stand-alone' version of the VGa interface. This will be a simple video game. Phase 2 will be the development of a 'stand alone' VGA controller using the experience gained in Phase 1. This controller will then be integrated with the Nios® CPU. The final step will be to write a simple C program to test the VGA controller.

Phase One:

The implementation of a simple version of the game of 'Pong'. This is a hardware only solution. Your starting point is the example, written in Verilog®[1], at

http://www.fpgas4fun.com/pong

Phase Two:

Rework your design in order to implement a VGA controller that reads the RGB data from 'video memory'. After testing and simulation, integrate your controller with the Nios processor system and write a simple 'C' program to use the new video interface. The information at
http://www.eecg.utoronto.ca/~singhd/241/vgacon.htm
may be used to support this phase. However you must be able to explain how you have reworked your initial model

Requirements:

To design and develop a hardware implementation of a VGA controller derived from the examples at

http://www.fpgas4fun.com/pong

and

http://www.eecg.utoronto.ca/~singhd/241/vgacon.htm

i) developed using an appropriate methodology,

ii) tested under simulation and

iii) implemented on the APEX™ evaluation board..

Deliverables:

- Complete design documentation showing requirements, references to standards documents that you have worked to, and the designs for your system (eg. UML, ASM, sequence enumeration etc).
- VHDL source code for your design. This must be well commented, in accordance with ESA VHDL Modelling Guidelines section 2.3.
- Documentation for your testing strategy.
- A brief (1 - 2 page) conclusion indicating successes, failures and future enhancments.
- Test results must be shown to your lab tutor.
- Hardware testing must be demonstrated in the lab.

[1] Verilog is an HDL with a 'C' style syntax

Marking Schema

Marks will be affected by :

- the quality of the documentation,
- evidence of a professional approach to the problem,
- quality of the design,
- implementation, verification and testing of your interface.

Evidence to support the above could include a record of design decisions and changes, code version control logs, data from the digital capture oscilloscope,etc.

Indicative Allocation of Marks

- Phase 1: design 10; implementation 20; demonstration 10;

- Phase 2: design 10; implementation 30; demonstration 10;

- Miscellaneous 10;

The allocation of marks is subject to modification in the event of technical problems with the equipment or software.