



MODULAR PROGRAMME
ASSESSED COURSE-WORK SPECIFICATION

Module Details:

Module Code: UFSEHH-30-2	Module Title: CPU Architecture & VHDL	
Module Leader: Nigel Gunton		
Module Tutors: Nigel Gunton Rob Williams		
Assignment CW2	Element Number: Weighting 25%	Total Assignment Time: 12 hrs

Dates:

Date assignment issued to students: wb February '04	Date for return of marked work: wb '04
Submission Place: post-box in N foyer, below the North stairs	Date of Submission: 1st April 04
	Time of Submission: 10.00am

Deliverables:

As listed on the Assignment spec sheet

Foreword

This assignment is the second part of a two part assignment. Work done for this assignment extends the work done during the first assignment. The minimum hand-in requirement for this phase is indicated below, along with the required demonstrations and discussions. This phase will include the integration of the ALU and the register set with the control unit to form a complete CPU. This design will then be extended by the addition of new instructions and registers.

You should work in pairs for this assignment. If this is not possible you must discuss the situation with your tutor.

Overview

Modern 'systems on silicon' may often require a complex control unit or sequencer. This can have similarities to the control unit of a simple CPU in that it has to generate a sequence of control signals dependent on the clock, current input condition and current 'instruction'. It is also possible that a design for a system is best implemented by a simple CPU like device without requiring the complexity of a third party CPU core as 'bought in' IP, or incurring the costs of devices with a CPU core already embedded in them.

The assignment will be supported by the lectures and support will be given in the lab sessions.

Details

- 1 If you have not already completed the coding and testing of your CPU control unit then you should consider this a priority as the rest of the assignment will utilize your control unit.
- 2 Develop and test the ALU as described in the first assignment specification and as discussed in the lectures.
- 3 Develop and test the various registers that are required by your design from semester 1.
- 4 Integrate the CU, the ALU and the registers into a CPU and test with the program that will be provided.
- 5 Select **ONE** of the following options :
 - a) Extend the instruction set and the register set to support a stack with branch and return instructions. Write a simple program to test your extended instruction set. Your modified processor should also pass the test from part 4).

or

- b) Create a complete System on Chip (SoC) with a small program in ROM and some RAM for storage. Test the complete system with a simple program that uses both `read` and `write` memory cycles.

The following should be done on an individual basis :

Control units can be divided into 2 types, 'hardwired' and micro-sequence. For the purposes of this assignment you have been developing a hardwired control unit. Having developed, and tested, the hardwired control unit for the 'Carpinelli RS-CPU'¹, you should consider how you might implement it as a micro-coded control unit.

- 6 Provide a report explaining how you would convert your hard-wired control unit into a microcoded control unit. You should provide diagrams to support your discussion. (A maximum of three A4 page plus diagrams.)

¹ From John Carpinelli's design for a relatively simple CPU

Deliverables

You **MUST** include a copy of your semester 1 work with the deliverables for this semester.

- i) The high level code and test results for parts 1 -3
 - Designs - 15 marks
- ii) The netlist for your CPU and test results for it.
 - CPU design & integration - 10 marks
 - Testing - 15 marks
- iii) The completed design and testing for either the SoC or the extended CPU
 - Design & coding - 20 marks
 - Testing & results - 20 marks
- iv) Your individual discussion
 - Report - 20 marks