



MODULAR PROGRAMME ASSESSED COURSE-WORK SPECIFICATION

Module Details:

Module Code: UQC149S2	Module Title: Embedded Systems on Silicon	
Module Leader: Nigel Gunton		
Module Tutors: Nigel Gunton		
Assignment	Element Number: Weighting	Total Assignment Time:
CW1	75%	20 hrs + lab time

Dates:

Date assignment issued to students: Oct 21st	Date for return of marked work: w/b 05/05/03
Submission Place: post-box in N foyer, below the North stairs	Date of Submission: w/b 07/04/03
	Time of Submission: 10.00am

**UQC149S2 Embedded Systems on Silicon
Assessed Coursework
October 2003**

This assignment must be delivered, with a completed Official Cover Sheet (available from N block) before 10:00 ??????????

Requirements:

To design and test the implementation of a microwave oven controller. The design should be developed initially as a finite state machine and then converted to VHDL. The microwave oven should support at least the following inputs and outputs as well as any others that you consider are required for the operation of a domestic microwave oven :

- a) Door open dector switch
- b) User Power select buttons, (min. 4 power settings)
- c) Interior light control
- d) Timer select (but see note below)
- e) Start Button
- f) Cancel Button

The behaviour of the system should be that expected of a domestic microwave oven. eg. Disabling the power when the door is opened etc.

A domestic microwave oven offers a good example of the class of designs that could be implemented either with software or using dedicated hardware. This assignment allows you to investigate and implement the controller using programmable logic devices.

The domestic microwave oven is not as simple as it looks. You will be expected to use your knowledge of software design methods such as UML and FSM as well as other techniques that will be presented in this module, namely sequence enumeration and ASM. This knowledge should inform your choice of methodology and you will be expected to justify your choice. The design phase of this assignment is not to be underestimated!

Your design **MUST** be signed off by a tutor before you start coding.

Deliverables:

Note that items 5 & 6 are provided for on the coursework checklist and must be signed off via this checklist.

- 1) A complete set of design documents that should include as a minimum
 - An overview of your system functionality (specification),
 - detailed designs with keys to the diagrams where appropriate,
 - justification of your design decisions and assumptions made.

20 marks
- 2) The VHDL code for your design. This must be well commented and accompanied with the version control logs that were kept during development. You may develop your VHDL code using any of the approaches that have been presented in this module but it must be clearly derived from your initial designs. Any deviation from your designs must be documented. Failure to provide change logs will incur a penalty of **-7 marks**.

25 marks
- 3) Testing must be thorough and should include
 - A written explanation of your testing strategy.
 - A set of test patterns, with comments and the resultant output file from the simulation of the behavioural model. These must be presented as waveforms.

15 marks
- 4) An oral walkthrough of your FSM code. This must be signed off by a tutor on the checklist.

5 marks

- 5) Demonstration of your microwave oven running in hardware. This must be signed off by a tutor on the attached checklist.

10 marks

- 6) Modification of the structural description of your code to include memory of the current power setting and a simple timer that accepts an input value and generates a stop signal.

25 marks

General Comments

Support will be provided in the lab sessions for coding issues and for tool use. It is expected that initially you will use the FSM subset of the language supported by the Alliance toolkit for the state machine coding and the `sxconv` tool for the conversion to Lattice compliant EDIF. Completion of the final part of the assignment will require use of the structural subset of the language

For the first part of the assignment you may assume that the timer is an external device that responds to the signals `start/stop` and provides a signal indicating that the time period is completed. You are not required to consider the programming of the timer for the first part of the design process.

If you intend to implement your design in hardware then you are constrained to a maximum of 8 inputs and 8 outputs to your system. Note that the meaning of the inputs can be state dependent.

You are not expected to implement phase 6 in hardware, although bonus marks will be awarded if you do. It will be sufficient to provide test pattern results from simulation.

Deliverables You are expected to complete the items above and to hand in :

- 1) The signed checklist
- 2) Your design documentation.
- 3) Your commented code (top level design) and change logs.
- 4) A written explanation of your testing strategy, <= 500 words.
- 5) Printouts of your test results as screen shots of the waveforms.
- 6) Design documentation and structural code for part 6. Where appropriate this should include schematic designs.

NB: Take account of the marks schedule provided to maximize the marks you gain from the assignment.

STUDENT NAME :

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Please hand this in with your documentation.

Coursework Checklist

1) Design Documentation sign-off (before coding) :

Lab Tutor Signature.....

2) VHDL source code for your FSM :

3) Test Patterns for simulation :

4) Walk-through of your FSM code:

Lab Tutor Signature.....

Demonstration of hardware implementation :

Lab Tutor Signature.....

Demonstration of extended design :

Lab Tutor Signature.....