



MODULAR PROGRAMME ASSESSED COURSEWORK SPECIFICATION

Module Details:

Module Code: uqc143h3	Module Title: VHDL for RTS	
Module Leader: Nigel Gunton		
Module Tutors: Nigel Gunton		
Assignment CW1	Element Number: Weighting 75%	Total Assignment Time: 15 hrs

Dates:

Date assignment issued to students: Feb 12th	Date for return of marked work: w/b May 26th
Submission Place: postbox in N foyer, below the North stairs	Date of Submission: w/b 5th May
	Time of Submission: 10.00am

Deliverables:

As listed on the Assignment spec sheet

Requirements:

To design and develop a hardware implementation from the list below. The design should be :-

- i) developed using an appropriate methodology, eg. Sequence Enumeration, ASM.
- ii) coded in VHDL, tested under simulation and, where appropriate,
- iii) programmed into a Lattice isp1016 or isp2032, followed by testing of the hardware.

The work should be undertaken in teams of two (2) or three (3).

The design problem should be taken from the following list. It may be possible to negotiate alternative design problems however they should have some 'timing issue' involved. Not all the problems are of the same size or complexity and this will be considered when assessment is made. It is expected that the smaller problems will be taken to the hardware stage whereas more complex problems may be either

- a designed, coded and tested in simulation *or*
- b designed but only a subcomponent is completed to hardware testing. Suitable sub-components must be agreed with the module leader.

Possible Design Problems

- **UPC Version A Bar Code Reader:** to be taken to the hardware stage.
- **ISA to 683xx interface.** Variable, eg. ISA Ethernet Controller is straight-forward, full ISA is more complex!
- **IBM Keyboard to 683xx interface.** Unknown complexity, excludes 683xx driver software.
- **I²C slave interface.** Fairly large.

Deliverables:

- Complete design documentation showing requirements, references to standards documents that you have worked to, and the designs for your system (eg. UML, FSM, sequence enumeration etc).
- VHDL source code for your design. This must be well commented, in accordance with ESA VHDL Modelling Guidelines section 2.3.
- Documentation for your testing strategy, test patterns and results. For hardware testing this **MUST** be demonstrated in the lab.
- A brief (1 - 2 page) conclusion indicating successes, failures and future enhancements.

Marking Schema

The exact marking scheme will be negotiated with each team and will be based on the anticipated breakdown of effort. For example a small design taken to hardware would be marked 30:30:30:10 for design, simulation, hardware, conclusions. A large design would be marked 45:45:10 for design, simulation, conclusions.

One third of the mark for the design will be allocated through peer review of team presentations.