Undergraduate Modular Program

UQC143H3 - VHDL for Real-Time Systems

**** 2001

BSc. Hons. Computing for Real-time Systems

Date:

Time:

Time allowed: 2 Hours plus 10 minutes reading time

Instructions to candidates:
1. You must attempt Section 1 and also answer any two questions from section 2.
2. All questions in each Section carry equal marks.
3. You are permitted to bring in up to 6 single-sided or 3 double-sided sheets of A4 notes based on the case study. These notes must be handed in with your script.

Special materials
NONE.
Section 1: Case Study : 60 marks

Assume use of the Alliance CAD system as used in the lab. sessions.

1) The testing, in both simulation and hardware, of this state machine can be considered to divide into at least three phases, for example :-

   • simulation of the VHDL description of the state machine with specified input sequences.
   • testing of the VHDL description of the state machine in a simulated environment.
   • testing of the hardware implementation.

   a) Discuss how you would approach the first phase of testing in the above list. Your answer should include consideration of the extent to which this would meet the constraints expressed in the case study. (10 Marks)

   b) Show how would you modify your VHDL model of the state machine in order to permit its testing in a simulated environment and as indicated in figure (1); ie. The next set of inputs to the system is generated by the interaction between the current action and a model of the environment in which the robot is embedded, rather than from a specific pattern file sequence.

       Your answer should, if possible, provide a labelled sketch of your system components and an outline VHDL entity description as well as a written description of your environment model.

![Diagram](1)

   (15 Marks)

2) The following should be derived from your case-study notes.

   a) Provide a state machine design for your mining robot. This may be in either fsm diagram form, state flow chart, or as a state transition table. (10 Marks)

   b) Provide a VHDL entity description for your design. (5 Marks)

   c) Discuss how you would approach the implementation of your design in VHDL. Pay particular consideration to the appropriateness of behavioral and/or structural models. (10 Marks)

3) Consider the maze fragment in figure (2) over-leaf. Discuss how your state machine would respond if it was in the position and orientation shown by the arrow. Indicate the sequence of state transitions and the relevant events and actions that would occur.

   Discuss the behaviour if NOT WL took precedence in the set of wall sensor inputs
End of Section One (1).
Section 2: 40 marks
Answer any two (2) questions from this section

4) A simple D-type flip-flop with preset and clear, is modeled behaviorally as follows and an initial test produces the waveform shown in figure (3).

architecture example of funny_d_type is

signal A, B, C, D, QI, QbarI : bit;
begins
A <= not(prst and D and B) after 1 ns;
B <= not(A and clear and clock) after 1 ns;
C <= not(B and clock and D) after 1 ns;
D <= not(C and clear and data) after 1 ns;
QI <= not(prst and B and QbarI) after 1 ns;
QbarI <= not(QI and clear and C) after 1 ns;
Q <= QI;
Q_bar <= QbarI;

figure (3)
a) Discuss possible reasons for the three events circled on the figure. The test-pattern file is provided in Appendix A: (15 Marks)
b) Briefly consider the issues that would need to be resolved when developing a structural model of this device at the gate level? (5 Marks)
5) The code in figure (4) provides a data-flow description of a simple combinational logic circuit.
   a) Provide a labelled gate level schematic design of this circuit suitable for implementing as a structural VHDL model. (5 Marks)
   b) Provide an alliance style input test-pattern for the data-flow description. Your input patterns should be at 1 nanosecond intervals and of at least 16 nanoseconds duration. It should also show transitions on at least the a and b inputs. (3 Marks)
   c) Briefly explain the term δ delay (delta delay) with respect to the simulation of behaviour VHDL. (2 Marks)
   c) Show, with the aid of diagrams and using your example test-pattern from 5.b, how a simulator would place transactions on signals from creation to expiry. Your example should show at least the first 6 milliseconds of your test-pattern and include transitions on inputs a and b. (10 Marks)

   entity gates is
      port (a, b, c : in bit; z : out bit);
   end gates;

   architecture data_flow of gates is
      signal w, x, y : bit;
   begin -- data_flow
      w <= not a after 2 ns;
      x <= a and b after 1 ns;
      y <= c and w after 1 ns;
      z <= x or y after 1 ns;
   end data_flow;

   figure (4)

6) Designers are increasingly using high level languages such as VHDL, followed by logic synthesis to develop systems. Implementation is achieved by using technologies such as ASICs, FPLDs or CPLDs.
   a) Discuss the issues facing a designer when using this approach to take a design from VHDL to the target hardware. You may use examples from your assignment work in your discussion. You should include consideration of the tools used. (15 Marks)
   b) Briefly discuss how the description and synthesis of a finite state machine in VHDL differs from a software description of a finite state machine in a language such as C. (5 Marks)
Appendix A:

in preset;
in clear;
in data;
in clk;
out Q;
out Q_bar;

#test file for q2 d-type
#no spy vbe
begin

< 0 ns> p: 01 0 0 ? **;
< +2 ns> p: 01 0 0 ? **;
< +2 ns> p: 01 0 1 ? **;
< +2 ns> p: 01 0 1 ? **;
< +2 ns> p: 11 0 0 ? **;
< +2 ns> p: 11 0 0 ? **;
< +2 ns> p: 11 0 1 ? **;
< +2 ns> p: 11 0 1 ? **;
< +2 ns> p: 10 0 0 ? **;
< +2 ns> p: 10 0 0 ? **;
< +2 ns> p: 10 0 1 ? **;
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< +2 ns> p: 11 1 0 ? **;
< +2 ns> p: 11 1 1 ? **;
< +2 ns> p: 11 1 1 ? **;
< +2 ns> p: 11 1 0 ? **;
< +2 ns> p: 11 1 0 ? **;
< +2 ns> P: 11 1 1 ? **;
end;